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EXAMINER	
FLOURNOY, HORACE L	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,036	RAMCHANDRAN, AMIT	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendments received 2/16/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-15 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-15,19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed February 16th, 2006. Claims 11-12, 14-16, 18-20 and 22 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments. Accordingly, this action has been made NON-FINAL.

Claim Rejections - 35 USC § 112 – 2nd paragraph

Claim 1 recites the limitation "the heterogeneous processing nodes" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10, and 12-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilson (U.S. Patent no. 5,557,734, hereafter referred to as Wilson).

Independent Claims

With respect to **independent claims 1 (and 12),**

"*A distributed data cache* **[disclosed, e.g. in FIG. 5, elements MEM0-MEM8]** *coupled to one of a plurality of reconfigurable execution nodes (RXN), wherein the heterogeneous processing nodes* **[disclosed in FIG. 5 Processors 46, 47, and 48]** *are coupled by a programmable interconnection network* **[disclosed, e.g. in column 1, lines 10 and 11]** *having a network root* **[FIG. 1, element 21, "Host"]** *and a plurality of crosspoint switches,* **[FIG. 5, elements 50, 51]** *the distributed data cache comprising: a plurality of cache memory units each* **[e.g. FIG. 5, element MEM8]** *having a plurality of cache ports; and a plurality of data buses connected with each of the cache memory units, wherein each of the plurality of data buses is connected with one of the plurality of cache ports of the cache memory units* **[As noted in FIG. 5, the cache memory MEM8 discloses two separate ports (plurality of cache ports) which are connected to two different data buses]**; *and the reconfigurable execution node adapted for processing data and having at least one data input and at least one data output, wherein the data input and data output are connected with the plurality of data buses."* **[As noted in FIG. 5, each of elements 46, 47, and 48 have at least one data input and one data output which are connected to a plurality of data buses]**

With respect to **independent claim 12**,

"An apparatus for transferring a plurality of data values arranged in a matrix, **[Wilson teaches this limitation, e.g. in column 31, lines 20-24]** *the apparatus coupled to one of a plurality of heterogeneous processing nodes,* **[disclosed in FIG. 5 Processors 46, 47, and 48]** *wherein the heterogeneous processing nodes are coupled by a programmable interconnection network* **[disclosed, e.g. in column 1, lines 10 and 11]** *having a network root* **[FIG. 1, element 21, "Host"]** *and a plurality of crosspoint switches,* **[FIG. 5, elements 50, 51]** *the apparatus comprising: a plurality of cache memory units,* **[disclosed, e.g. in FIG. 5, elements MEM0-MEM8]** *each cache memory unit having a plurality of cache ports; and a plurality of data buses, each data bus connected with a different one of the plurality of cache ports from each of the cache memory or register file units."* **[As noted in FIG. 5, the cache memory MEM8 discloses two separate ports (plurality of cache ports) which are connected to two different data buses]**

With respect to **independent claim 20**,

"A method for transferring a plurality of data values arranged in a matrix to transpose the matrix, **[Wilson teaches this limitation, e.g. in column 31, lines 20-24]** *the matrix including a plurality of heterogeneous processing nodes* **[disclosed in FIG. 5 Processors 46, 47, and 48]** *coupled by a programmable interconnection network* **[disclosed, e.g. in column 1, lines 10 and 11]** *having a*

network root **[FIG. 1, element 21, "Host"]** *and a plurality of crosspoint switches,* **[FIG. 5, elements 50, 51]** *the method comprising: retrieving a first subset of data values from the plurality of data values from a memory unit storing the matrix in rows;* **[Wilson discloses in column 15, lines 18-20, "...the four cache memories MEM5-MEM8 are capable of storing arbitrary segments of matrix data retrieved from external memory 23." Wilson teaches retrieving a first subset of data values from the plurality of data values (arbitrary segments of matrix data) from a memory unit (external memory).]** *simultaneously transferring the first subset of data values comprising one of the rows of the matrix; to a plurality of data buses, wherein each data value of the first subset is transferred to a different one of the plurality of data buses;* **[Wilson next discloses in the abstract "The system further includes a controller for each chip that sequences a burst of consecutive rows of a data matrix from the external cache burst memory, to be stored in either the cache memory associated with each of the processing units or routed directly to the processors included in each processing unit." In this disclosure, Wilson teaches the simultaneous transfer of the first subset of data values (burst of consecutive rows of a data matrix) to a plurality of data buses (routed directly to the processors included in each processing unit). Since there is a different data bus connected to the plurality of processing units (see FIG. 1) the plurality of data values are each transferred to a different one of the plurality of buses (that lead to the different processing units).]**

simultaneously loading the first subset of data values from the plurality of data buses to a first cache memory unit having a plurality of cache ports, wherein each cache port receives a data value from a different one of the plurality of data buses to define a column of the matrix; and repeating the operation for each row of the matrix to complete transposing of the matrix." **[Wilson also teaches simultaneously loading the first subset of data values from the plurality of data buses to a first cache memory unit (...to be stored in either the cache memory associated with each of the processing units). The examiner interprets loading to mean stored. It is inherent for a cache memory unit to have a plurality of cache lines when there are pluralities of data values stored within the cache. FIG. 5 shows each cache port (see cache memory units MEM0-8) receiving data from a different one of the plurality of data buses (shown in Transpose In Bus connecting to the cache memory units through S10-17).]**

Dependent Claims

With respect to **claim 3**,

"The distributed data cache of Claim 1, further comprising a multiplexer for alternately connecting the data input with each of the plurality of data buses" is disclosed in column 14, lines 64-65.

The examiner interprets this claim to mean that the distributed data cache of claim 1 comprises a multiplexer for connecting data input with each of the plurality of buses.

Wilson discloses in column 14, lines 64-65, FIG. 7, elements 71-72, "The data line 74, which is the output from multiplexer 73, and data line 59, provided as inputs to multiplexer 75..." FIGs. 5 and 7 disclose how the data is connected to the plurality of buses

With respect to **claim 4**,

"The distributed data cache of Claim 1, further comprising a multiplexer for alternately connecting the data output with each of the plurality of data buses" is disclosed in column 14, lines 64-65.

The examiner interprets this claim to mean that the distributed data cache of claim 1 comprises a multiplexer for connecting data output with each of the plurality of buses.

Wilson discloses in column 14, lines 64-65, FIG. 7, element 75, "The data line 74, which is the output from multiplexer 73, and data line 59, provided as inputs to multiplexer 75..." FIGs. 5 and 7 disclose how the data is connected to the plurality of buses.

With respect to **claim 5**,

"The distributed data cache of Claim 1, further comprising a plurality of data address generators connected with a memory unit and the plurality of data buses without latency" is disclosed in column 24, lines 39-46.

The examiner interprets this claim to mean the distributed data cache of Claim 1, which further comprises a plurality of data address generators connected with a memory unit and the plurality of data buses. The examiner interprets this claim sans the limitation "without latency" for reasons stated above.

Wilson discloses "The word on .lines CTL12 correspond to a starting address. The output on line 103 is sent to the address inputs of all cache memories MEMS-MEMS. Control lines CTL13 provides a word, which is constant for this data cycle, that is added to the output of counter 121 by adder 126, which then outputs an address for memories MEM0-MEM4" (column 24, lines 39-46).

With respect to **claims 6 and 7**,

"The distributed data cache of Claim 5, wherein the plurality of data address generators are adapted to retrieve a plurality of data values from the memory unit and communicate the plurality of data values to the plurality of data buses directly without any latency due to registering" and "The distributed data cache of Claim 6, wherein the plurality of data address generators are adapted to

simultaneously communicate the plurality of data values to the plurality of data buses, wherein each of the plurality of data values is communicated to a different one of the plurality of data buses," respectively are both disclosed in column 26, lines 26-33, FIG. 13 element 24C. **[Wilson discloses "The data is burst in sequential row order, or, in other words, a row at a time, wherein each clock pulse to external memory 23 causes the next consecutive address (e.g., the next row of data in memory 23) to be referenced, the data stored therein being sent via lines 24C to, for example, the cache memories MEM0-MEM8, or to processors 46, 47, and 48 for processing during that clock cycle" is disclosed in column 26, lines 26-33, FIG. 13 element 24C. Wilson references (communicates or retrieves) a row of data (plurality of data values) to a plurality of data buses (lines 24C of FIG. 13) simultaneously (burst and during the same clock cycle).]**

With respect to **claim 8**,

"The distributed data cache of Claim 7, wherein the first cache memory unit is adapted to simultaneously load a plurality of data values from the plurality of data buses, such that each of the plurality of data values is loaded in a different one of the plurality of cache lines of the first cache memory unit through the same port" is disclosed in column 2, lines 44-48 and the abstract

The examiner interprets this claim to mean the cache memory units (MEM0-8 elements of FIG.5) can be made to simultaneously load (burst) one of

the sets of data values (one of a consecutive row of a data matrix) from the plurality of data buses (Note: both Transpose In and Transpose Out Buses shown in FIG. 5 of Wilson are each a plurality of buses). Additionally, the apparatus can be made to load a data value to a different one (of a plurality of) cache lines of the first cache memory unit through the same port.

Wilson discloses "The system further includes a controller for each chip that sequences a burst of consecutive rows of a data matrix from the external cache burst memory, to be stored in either the cache memory associated with each of the processing units or routed directly to the processors included in each processing unit" (abstract). Wilson also discloses in column 2, lines 44-48, "Usage of cache memory internal to the microprocessor allows instructions and data to be stored in different caches and be simultaneously addressed thereby improving the memory bandpass internally." Since data is stored in different caches, it is transferred through a plurality of buses. Also, FIG. 1 shows since different caches are addressed simultaneously, there are different cache lines through which data values are loaded in (stored).

With respect to **claim 10**,

"The distributed data cache of Claim 1, further comprising at least one additional cache memory unit also having a plurality of cache lines, wherein each cache line of the additional cache memory unit is connected with the plurality of data buses," is disclosed in column 20, lines 54-59.

The examiner interprets this claim to mean (the distributed data cache of Claim 1) which comprises at least one additional cache memory unit that also has a plurality of cache lines, wherein each cache line of the additional cache memory unit is connected with the plurality of buses. It is inherent that a cache memory unit has a plurality of cache lines.

Wilson discloses in column 20, lines 54-59, FIG. 5 "As shown in FIG. 5, each of the eight transpose-bus-out lines 55 are connected via a respective line 100 to a respective output selector S56 in each of the processing units 29A-29H. Control line CTL3 in only a selected one of the eight processing units 29A-29H can be activated to cause the contents of the respective cache memories MEM0-MEM7 to be transferred to transpose-bus-out 55 via selectors S10-S17." Wilson teaches in FIG. 5 that each of the cache memory units' (at least one additional cache memory unit: see elements MEM0-8) cache lines (inherent) is connected with the plurality of data buses (transpose out/in buses through element S10-17 and S20-28).

With respect to **claim 14**,

"The apparatus of Claim 13, wherein the plurality of data values comprises a plurality of sets of data values" is disclosed in column 5, lines 64-66 and column 8 lines 51-53.

The examiner interprets this claim to mean a plurality of data values comprises a plurality of sets or groups of data values. Wilson outlines a

"respective row of N data bits" in column 5, lines 64-66. Wilson shows that data is grouped over a plurality of rows (set of data values). Wilson also discloses "one or more columns of array data stored in memory" in column 8, lines 51-53, which illustrate a set of data values (one or more columns of array data).

(Note: The following is in regard to claims 13, 15)

With respect to **claim 13**,

"The apparatus of Claim 12, further comprising a plurality of data address generators adapted to retrieve a plurality of data values from the memory unit and communicate the plurality of data values to the plurality of data buses, the apparatus being configured to transpose a matrix stored in the main memory by reading a matrix comprising a plurality of row elements from the main memory into the plurality of data buses, then simultaneously transferring the row elements to the cache ports of one of the cache memories, and repeating the operation for each row of the stored matrix." **[disclosed, e.g. in column 11, lines 37-56. Also see FIGs. 5 and 10 as well as all related text within the specification]**

With respect to **claim 15**,

"The apparatus of Claim 14, wherein the plurality of data address generators are adapted to sequentially communicate the plurality of sets of data values with the plurality of data buses without any register latency," **[As per claim 15, Wilson teaches that the data is burst in sequential row order, or, in other words, a**

row at a time (sequentially and in "data sets" or rows), and later sent via lines 24C (communicated to a plurality of buses).]

With respect to **claim 19**,

"The apparatus of Claim 16, wherein each of the cache memory units is adapted to simultaneously load one of the sets of data values from the plurality of data buses, such that each data value of the set of data values is loaded in a different one of the plurality of cache ports of the cache memory unit or register file" is disclosed column 2, lines 44-48 and the abstract.

The examiner interprets this claim to mean the cache memory units (MEM0-8 elements of FIG.5) can be made to simultaneously load (burst) one of the sets of data values (one of a consecutive row of a data matrix) from the plurality of data buses (Note: both Transpose In and Transpose Out Buses shown in FIG. 5 of Wilson are each a plurality of buses). Additionally, the apparatus can be made to load a data value from a set of data values to a different one of the plurality of cache memory units. As stated supra, the examiner interprets cache port to simply identify the means through which a data bus connects to a cache memory unit.

Wilson discloses "The system further includes a controller for each chip that sequences a burst of consecutive rows of a data matrix from the external cache burst memory, to be stored in either the cache memory associated with each of the processing units or routed directly to the processors included in each

processing unit" (abstract). Wilson also discloses in column 2, lines 44-48, "Usage of cache memory internal to the microprocessor allows instructions and data to be stored in different caches and be simultaneously addressed thereby improving the memory bandpass internally." Since data is stored in different caches, it is transferred through a plurality of buses. Also, since different caches are addressed simultaneously, there are different cache ports through which data values are loaded in (stored).

With respect to **claim 21**,

"The distributed data cache of claim 1, wherein the RXN includes a plurality of selectively configurable elements each having a configuration determined by the value of a multi-bit control word, the bits being simultaneously supplied in one or more of the control words stored in the cache memory units over the data buses."**[disclosed, e.g. in column 15, lines 35-55]**

With respect to **claim 22**,

"The distributed data cache of claim 21, wherein the RXN is adapted to be reconfigured to perform a sequence of operations responsive to a sequence of the control words." **[disclosed, e.g. in column 25, lines 4]**

With respect to **claim 23**,

> "The distributed data cache of claim 22, wherein each of the memory units comprises a plurality of cache lines, each cache line being associated with one of the plurality of cache ports, each cache line storing one of the control words, the sequence of control words being retrieved by an index uniquely identifying the cache line, a sequence of the indexes defining a single access control word." **[disclosed, e.g. in column 19, lines 59-67. The examiner notes that this limitation is anticipated by cache *burst* teachings.]**

With respect to **claim 24**,

> "The distributed data cache of claim 23, wherein the access control word is identified by a flag bit, the remainder of the access control word comprising a sequence of indexes." **[disclosed, e.g. in column 19, lines 59-67. The examiner notes that this limitation is anticipated by cache *burst* teachings.]**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 9 is rejected under 35 U.S.C. 103(a) as being obvious over Wilson (U.S. Patent no. 5,557,734) in view of Okuda et. al (US Patent No. 6,535,452 hereafter referred to as Okuda).

With respect to claim 9, Wilson teaches "The distributed data cache of Claim 1..." as stated supra.

Wilson, however, does not disclose expressly "...wherein the number of cache lines of the first cache memory unit are equal to the number of data buses."

Okuda discloses, "...respective blocks of the memory blocks corresponding to the m respective data pins, and are simultaneously activated, the activation of any one of the address selection lines connecting the data bus lines to a corresponding one of the m respective blocks and resulting in the n data pieces being input/output to/from the corresponding one of the m respective blocks" (Okuda abstract). The examiner interprets cache lines as memory blocks corresponding to respective data pins.

Wilson and Okuda are analogous art because they are from the same field of endeavor, that being cache or memory data distribution.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a distributed data cache of claim 1 in which the number of cache lines or memory blocks of the cache memory unit is equal to the number of data buses outlined above to arrive at claim 9.

The motivation for doing so would have been obvious based on the enhancement of speed of memory access, which is disclosed in column1, lines 32-42, which recites, "For the purpose of speeding up the operation speed of semiconductor memory devices, generally, the operation of core circuits inside the memory devices need to be made faster. It is difficult, however, to speed up the operation of core circuits because of limitations such as wire delays. When a fixed number of data bits are to be serially input/output upon a single access, provision may be made not only to read data corresponding to the plurality of DQ pins in parallel from the memory core, but also to read serially output data in parallel from the memory core."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Wilson and Okuda before him/her to combine Okuda with Wilson for the benefit of having the number of cache lines equal to the number of data buses to obtain the invention as specified in claim 9.

Claim 11 is rejected under 35 U.S.C. 103(a) as being obvious over Wilson (U.S. Patent no. 5,557,734) with "Computer Organization and Design" 2nd edition, by Hennessy and Patterson offered as extrinsic evidence (hereafter referred to as Hennessy).

With respect to claim 11, Wilson teaches "The distributed data cache of Claim 10..." as stated supra.

Wilson, however, does not disclose expressly "...wherein the total number of cache memory units is equal to the number of cache lines in each cache memory unit."

Hennessy discloses, "In a set-associative cache, there are a fixed number of locations (at least two) where each block can be placed; a set-associative cache with n locations for a block is called an n-way set-associative cache. An n-way set-associative cache consists of a number of sets, each of which consists of n blocks..."(page 569). Blocks in this definition is analogous to cache line.

Wilson and Hennessy are analogous art because they are from the same field of endeavor, that being ordering or controlling memory commands.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to design a distributed data cache which has an N-way, M-line set associative cache design implementation wherein N is equal to M outlined above to arrive at claim 11. Each cache way is treated like a small direct mapped cache. The examiner interprets figures 6 and 7 to teach an implementation of a direct-mapped cache.

The motivation for doing so would have been obvious based on Hennessy, page 570, "The advantage of increasing the degree of associativity is that it usually decreases the miss rate..."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Wilson and Hennessy before him/her to

combine Hennessy with Wilson for the benefit of having a M-way, M-set associative distributed data cache to obtain the invention as specified in claim 11.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1ST POINT OF ARGUMENT:

With respect to the arguments on page 7 of the applicant's remarks and as per claim 1, the examiner believes that data busses that even passively move data from a cache memory to a node in fact comprises processing data.

As per claim 3, the multiplexers of FIG. 7 show the functionality of alternately connecting a data input with each of the plurality of data buses and therefore anticipates the claim language of claim 3. The truth table processor, element 46 of FIG. 5 which is embodied in detail in FIG. 7, connects with the plurality of data buses as shown in FIG. 5.

As per claim 12, FIG. 5 does indeed show a plurality of cache memory units, as shown in column 11, line 43. Each cache memory (MEM0-8) shows a plurality of ports connected to it as shown in FIG.5. Each cache memory is connected to both the Transpose Out and Transpose In buses as shown in FIG.5.

With respect to the arguments on page 8 of the applicant's remarks and as per claims 7 and 8, the examiner apologizes for any confusion regarding cache memory units MEM0-8. Each of the memory units are duplicates with identical functionality. Therefore each rejection stated by the examiner supra

which references a particular memory unit (e.g. MEM8) can be replaced with another memory unit (e.g. MEM0).

Finally, with respect to the arguments regarding claim 20, refer to the point of argument above with respect to claim 3 as well as column 26, lines 60-64.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have

questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon

Reginald G. Bragdon

HLF
April 1st, 2007

Supervisory Patent Examiner
Technology Center 2100